L Number	Hits	Search Text	DB	Time stamp
1	316	438/637,623,700,710,725,780,798.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)	USPAT; US-PGPUB	2002/08/23 13:29
2	288	(438/637,623,700,710,725,780,798.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)) and (via or hole or opening or recess or trench)	USPAT; US-PGPUB	2002/08/23 13:30
3	279	((438/637,623,700,710,725,780,798.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)) and (via or hole or opening or recess or trench)) and @ad<=20010828	USPAT; US-PGPUB	2002/08/23 13:30
4	95	(((438/637,623,700,710,725,780,798.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)) and (via or hole or opening or recess or trench)) and @ad<=20010828) and RF	USPAT; US-PGPUB	2002/08/23 13:31
5	90	257/642,774,758.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)	USPAT; US-PGPUB	2002/08/23 13:30
6	83	(257/642,774,758.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)) and (via or hole or opening or recess or trench)	USPAT; US-PGPUB	2002/08/23 13:30
7	71	((257/642,774,758.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)) and (via or hole or opening or recess or trench)) and @ad<=20010828	USPAT; US-PGPUB	2002/08/23 13:30
8	23	(((257/642,774,758.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)) and (via or hole or opening or recess or trench)) and @ad<=20010828) and RF	USPAT; US-PGPUB	2002/08/23 13:31

DOCUMENT-IDENTIFIER: US 20010046781 A1

TITLE: Method for etching organic film, method for fabricating semiconductor device and pattern formation method

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An organic film is etched by using **plasma** generated from an **etching** gas containing a first gas including a straight chain saturated hydrocarbon and a second gas including a nitrogen component.

[0002] For the purpose of increasing the operation speed and lowering the consumption power of semiconductor devices, decrease of the dielectric constant of an interlayer insulating film included in a multi-level interconnect structure is recently regarded as significant. In particular, an **organic** film with a small dielectric constant can be easily formed by spin coating and curing, and hence is regarded as a very promising interlayer insulating film of the next generation. A well known example of the **organic** film with a small dielectric constant is an **organic** film including an aromatic **polymer** as a base.

[0003] In order to fabricate a device with a refined design rule of a gate length of 0.18 .mu.m or less, a fine line processing technique of approximately 0.25 .mu.m or less is necessary, and the design rule is considered to be more and more refined in the future. An organic film is generally patterned by **plasma etching,** but a fine pattern of 0.25 .mu.m or less is very difficult to form from an organic film.

[0004] Known examples of the **plasma etching** employed for an organic film are a process using an **etching** gas including a N.sub.2 gas and a H.sub.2 gas as principal constituents (reported by M. Fukusawa, T. Hasegawa, S. Hirano and S. Kadomura in "Proc. Symp. Dry Process", p. 175 (1998)) and a process using an etching gas including a NH.sub.3 gas as a principal constituent (reported by M. Fukusawa, T. Tatsumi, T. Hasegawa, S. Hirano, K. Miyata and S. Kadomura in "Proc. Symp. Dry Process", p. 221 (1999)).

[0005] One of conventional **etching** methods will now be described as Conventional Example 1 referring to the result obtained by **etching** an organic film with a magnetic neutral loop discharge (NLD) **plasma etching** system manufactured by Ulvac Corporation ("SiO.sub.2 **Etching** in magnetic neutral loop discharge **plasma**", W. Chen, M. Itoh, T. Hayashi and T. Uchida, J. Vac. Sci. Technol., A16 (1998) 1594).

[0007] **Plasma etching** system: NLD **plasma etching** system Volume flow ratio per minute in standard condition of **etching** gas:

[0016] FIGS. 14A and 14B show states where an organic film 105 formed on a semiconductor substrate 104 is subjected to **plasma etching** by using a mask pattern 106 of, for example, a silicon oxide film formed on the organic film 105. FIG. 14A shows a state in the middle of the **plasma etching** and FIG. 14B shows a state after completing the **plasma etching**. In FIGS. 14A and 14B, a reference numeral 107 denotes a first recess having a small diameter and a reference numeral 108 denotes a second recess having a comparatively large diameter. Although not shown in the drawings, a metal material film is formed

over the mask pattern 106 so as to fill the first recess 107 and the second recess 108, and a portion of the metal material film formed on the mask pattern 106 is removed by, for example, chemical mechanical polishing (CMP), so as to form a connection plug or a metal interconnect from the metal material film.

[0021] In the three-layer resist process, after an organic film and a silicon oxide film are successively formed on a semiconductor substrate, a thin resist pattern is formed on the silicon oxide film. Then, the silicon oxide film is subjected to **plasma etching** by using the resist pattern as a mask, so as to form an oxide film pattern by transferring the resist pattern onto the silicon oxide film. Next, the organic film is subjected to dry development (**plasma etching**) by using the oxide film pattern. Thus, a fine organic film pattern having a high aspect ratio is formed from the organic film.

[0024] **Plasma etching** system: NLD **plasma etching** system

[0041] In Conventional Example 3, the dry development is carried out on the organic film through the **plasma etching** using the **etching** gas including an O.sub.2 gas as a principal constituent. Therefore, as is shown in FIGS. 16A and 16B, the hole formed in the organic film pattern 110 has a diameter larger than the diameter of an opening of the oxide film pattern 109, and the hole formed in the organic film pattern 110 has a bowing cross-section. When the etch target film is etched by using the organic film pattern 110 with the hole having such a bowing cross-section, it is difficult to highly precisely conduct the etching.

[0049] In order to achieve the first object, the method for **etching** an organic

film of this invention comprises a step of **etching** an organic film by using **plasma** generated from an **etching** gas containing a first gas including a straight chain saturated hydrocarbon and a second gas including a nitrogen component.

[0050] In the present method for **etching** an organic film, an organic film is etched by using **plasma** generated from the mixed gas containing the gas including a hydrocarbon and the gas including a nitrogen component. Therefore, a deposition film is formed on an etch target surface, and owing to the deposition film, an ion assisted reaction is caused on the bottom of a recess substantially without depending upon the aspect ratio. Accordingly, a constant etching rate can be obtained without depending upon the aspect ratio, namely, the diameter of the recess.

[0059] The method for fabricating a semiconductor device of this invention comprises the steps of forming an organic film on a semiconductor substrate; forming, on the organic film, a mask pattern including an inorganic compound as a principal constituent; and forming a recess in the organic film by selectively **etching** the organic film by using the mask pattern and by using **plasma** generated from an **etching** gas containing a first gas including a straight chain saturated hydrocarbon and a second gas including a nitrogen component.

[0060] In the present method for fabricating a semiconductor device, an organic film is etched by using **plasma** generated from the mixed gas containing the gas including hydrocarbon and the gas including a nitrogen component, namely, a semiconductor device is fabricated by the present method

for **etching** an organic film. Therefore, a recess with a vertical or forward taper cross-section can be formed in the organic film with a very small RIE lag characteristic.

[0070] The pattern formation method for this invention comprises the steps of forming an organic film on a substrate; forming, on the organic film, a mask layer including an inorganic component; and forming an organic film pattern from the organic film by selectively **etching** the organic film by using the mask layer and by using **plasma** generated from an **etching** gas containing a first gas including a straight chain saturated hydrocarbon and a second gas including a nitrogen component.

[0071] In the present pattern formation method, the organic film pattern is formed by conducting selective **etching** on the organic film by using **plasma** generated from the **etching** gas containing the gas including a straight chain saturated hydrocarbon and the gas including a nitrogen component, namely, the organic film pattern is formed by the method for **etching** an organic film of this invention. Therefore, an opening formed in the organic film pattern can be prevented from having a larger dimension than an opening of the mask layer, and an opening with a vertical or forward taper cross-section can be formed in the organic film pattern with a very small RIE lag characteristic. Accordingly, a mask pattern can be highly precisely formed with a large process margin.

[0100] In the method for **etching** an organic film of Embodiment 1, a mixed gas including, as principal constituents, a CH.sub.4 gas and a N.sub.2 gas is used as the **etching** gas, so as to etch an organic film with

plasma generated from
the mixed gas. Exemplified etching conditions in
Embodiment 1 are:

[0101] **Plasma etching** system: NLD **plasma etching** system
Type of **etching** gas and
flow rates per minute in standard condition:

[0121] In general, in conducting anisotropic **etching** by
using **plasma, the**
etching is mainly realized by proceeding an ion assisted
etching reaction, and
is minimally proceeded by chemical sputtering, physical
sputtering and a
thermochemical reaction as compared with the ion assisted
etching reaction. In
the ion assisted reaction, when ions are released from the
plasma to reach an
etch target film, the ions are accelerated by an electric
field of a plasma
sheath region formed between a plasma generation region and
the etch target
film so as to collide with the etch target film, resulting
in proceeding a
surface chemical reaction in the vicinity of collision
portions by collision
energy. The mechanism of the etching through the ion
assisted reaction is
roughly divided into the following two types:

[0130] Accordingly, the **etching** reaction occurring on the
etch target surface
on the bottom of the recess is probably dominantly a
reaction to etch a small
amount of atoms or molecules adhered onto the etch target
surface and atoms
present on the surface of the organic film by the ion
assisted reaction caused
by the ions emitted from the **plasma** (by the mechanism of
the first case of the
first **etching** mechanism), or an **etching** reaction between
the ions and the etch
target surface (by the second **etching** mechanism). In
particular, in the
etching by using the conventional **plasma** of N.sub.2 and
H.sub.2, the **etching** is

probably dominantly proceeded by the second **etching** mechanism.

[0147] In the method for **etching** an organic film of this embodiment, a mixed gas including, as principal constituents, a CH.sub.4 gas and a NH.sub.3 gas is used as the **etching** gas, so as to etch an organic film with **plasma** generated from the mixed gas. Exemplified etching conditions in Embodiment 2 are:

[0148] **Plasma etching** system: NLD **plasma etching** system Type of **etching** gas and flow rates per minute in standard condition:

[0159] In the method for **etching** an organic film of Embodiment 3, a mixed gas including, as principal constituents, a CH.sub.4 gas, a N.sub.2 gas and a H.sub.2 gas is used as the **etching** gas, so as to etch an organic film with **plasma** generated from the mixed gas. Exemplified etching conditions in Embodiment 3 are:

[0160] **Plasma etching** system: NLD **plasma etching** system Type of **etching** gas and flow rates per minute in standard condition:

[0171] In the method for **etching** an organic film of Embodiment 4, a mixed gas including, as principal constituents, a CH.sub.4 gas, a N.sub.2 gas and a CH.sub.3NH.sub.2 (methylamine) gas is used as the **etching** gas, so as to etch an organic film with **plasma** generated from the mixed gas. Exemplified etching conditions in Embodiment 4 are:

[0172] **Plasma etching** system: NLD **plasma etching** system

[0178] Now, an effect of the method for etching an organic film of Embodiment 4 will be described in contradiction to etching of an organic film by using an

etching gas including a CH.sub.3NH.sub.2 gas as a principal constituent (in a flow rate per minute in the standard condition of the CH.sub.3NH.sub.2 gas of 100 ml) and etching of an organic film by using an etching gas including a CH.sub.4 gas and a N.sub.2 gas as principal constituents (in a ratio in the flow rate per minute in the standard condition between CH.sub.4 and N.sub.2 of 30 ml:70 ml). The **plasma etching** system, the antenna power, the bias power, the pressure and the substrate cooling temperatures are the same in all the **etching** as those employed in Embodiment 4.

[0196] In the method for **etching** an organic film of Embodiment 5, a mixed gas including, as principal constituents, a CH.sub.4 gas, a N.sub.2 gas and a rare gas (such as an Ar gas) is used as the **etching** gas, so as to etch an organic film with **plasma** generated from the mixed gas. Exemplified etching conditions in Embodiment 5 are:

[0197] **Plasma etching** system: NLD **plasma etching** system

[0207] When a rare gas is mixed in the **etching** gas, partial pressures in the **plasma of the etching** gas and atoms or molecules dissociated from the **etching** gas can be lowered in the vicinity of the inner walls of the reaction chamber, and hence, the deposition rate of the deposition is lowered. From this point of view, any of He, Ne, Ar, Kr, Xe and Rn may be used as the rare gas.

[0208] Furthermore, when a rare gas is mixed in the **etching** gas, the mixed rare gas is ionized in the **plasma**, and the ions of the rare gas are accelerated by a **plasma** sheath electric field formed in the vicinity of the inner walls of the reaction chamber so as to collide with the inner walls of the reaction chamber.

Therefore, the deposition deposited on the inner walls of the reaction chamber
is removed through physical sputtering. From this point of view, any of Ne,
Ar, Kr, Xe and Rn may be used as the rare gas. Since He is small in its
inertial mass, it cannot effectively remove the deposition through the physical
sputtering.

[0218] Now, as the premise of the description of the reason why a straight
chain saturated hydrocarbon exhibits the effects in the **etching** according to
any of Embodiments 1 through 5, dissociation of a molecule proceeded in **plasma**
will be examined.

[0219] In order to practically supply a gas to a **plasma etching** system, it is
necessary to generate a vapor pressure minimally required for enabling a mass
flow at 1 atm and room temperature. For this purpose, in a molecule
represented by C.sub.xH.sub.y (wherein x and y are positive integers), it is
effective that x is equal to or smaller than approximately 5.

[0228] A gas used in the **plasma etching** can be optimally selected basically
depending upon the method or system for exciting the **plasma**. As a plasma
system can more highly excite the plasma, a higher molecular weight gas can be
used, and hence, a gas to be used can be selected from a larger range.
Specifically, when a **plasma etching** system capable of high excitement, such as
an inductively coupled **plasma etching** system, a surface wave **plasma etching**
system, an NLD **plasma etching** system, a capacity coupled parallel plate **etching**
system using RF and an ECR **plasma etching** system, is used, a gas to be used can
be selected in accordance with the actually used power (energy).

[0231] Also, the effects of this invention are described in each of Embodiments 1 through 5 on the basis of the result obtained by using the **etching** gas in the NLD **plasma etching** system. However, the method for **etching** an organic film of any of Embodiments 1 through 5 is applicable to use of any **plasma etching** system, such as a parallel plate reactive ion **etching** system, a narrow-gap or two-frequency type parallel plate reactive ion **etching** system, magnetron enhanced reactive ion **etching** system, an inductively coupled **plasma etching** system, an antenna coupled **plasma etching** system, an electron cyclotron resonance **plasma etching** system and a surface wave **plasma etching** system.

[0235] Next, after forming a resist pattern 17 on the silicon oxide film 16 by a know lithography technique as is shown in FIG. 9C, the silicon oxide film 16 is subjected to **plasma etching** (dry **etching**) by using the resist pattern 17 as a mask, thereby forming a mask pattern 16A from the silicon oxide film 16 as is shown in FIG. 10A. The type of **etching** gas to be used in the **plasma etching** is not herein specified, and a gas including fluorocarbon may be used.

[0236] Then, the organic film 15 is subjected to **plasma etching** using **plasma** generated from the **etching** gas used in the **etching** method for any of Embodiments 1 through 5, namely, an **etching** gas including, as a principal constituent, a mixed gas of a molecule including carbon and hydrogen and a molecule including nitrogen, and by using the resist pattern 17 and the mask pattern 16A as masks. In this manner, recesses 18 each having a vertical or forward taper cross-section to be used as a via hole or an

interconnect groove
are formed in the organic film 15 as is shown in FIGS. 10B and 10C. This
etching is carried out under etching conditions of any of Embodiments 1 through
5. Since the resist pattern 17 is made from an organic compound, it is removed
during the etching of the organic film 15.

[0254] Next, the organic film 22 is subjected to **etching** by using **plasma**
generated from the **etching** gas used in the **etching** method for any of
Embodiments 1 through 5, namely, the **etching** gas including, as a principal
constituent, a mixed gas of a molecule including carbon and hydrogen and a
molecule including nitrogen, by using the silylated layer 28 as a mask. Thus,
openings 29 are formed in the organic film 22 as is shown in FIGS. 12A and 12B.

1. A method for **etching** an organic film comprising a step of **etching** an
organic film by using **plasma** generated from an **etching** gas containing a first
gas including a straight chain saturated hydrocarbon and a second gas including
a nitrogen component.

6. A method for fabricating a semiconductor device comprising the steps of:
forming an organic film on a semiconductor substrate; forming, on said organic
film, a mask pattern including an inorganic compound as a principal
constituent; and forming a recess in said organic film by selectively **etching**
said organic film by using said mask pattern and by using **plasma** generated from
an **etching** gas containing a first gas including a straight chain saturated
hydrocarbon and a second gas including a nitrogen component.

12. A pattern formation method comprising the steps of: forming an organic

film on a substrate; forming, on said organic film, a mask layer including an inorganic component; and forming an organic film pattern from said organic film by selectively **etching** said organic film by using said mask layer and by using **plasma** generated from an **etching** gas containing a first gas including a straight chain saturated hydrocarbon and a second gas including a nitrogen component.

	U	1 [1]	Document ID	Issue Date	Pages
1	☐	☒	US 20010012690 A1	20010809	12
2	☐	☒	US 20010005635 A1	20010628	8
3	☐	☒	US 20010005632 A1	20010628	17
4	☐	☒	US 20010004552 A1	20010621	18
5	☐	☒	US 6429122 B2	20020806	12
6	☐	☒	US 6410424 B1	20020625	14
7	☐	☒	US 6399511 B2	20020604	17
8	☐	☒	US 6352921 B1	20020305	10
9	☐	☒	US 6319822 B1	20011120	10
10	☐	☒	US 6114253 A	20000905	7

	Title	Current OR	Current XRef
1	Optimized metal etch process to enable the use of aluminum plugs	438/637	438/688
2	Ashing method and method of producing wired device	438/710	438/712
3	Dry etching method and semiconductor device manufacturing method	438/689	438/710; 438/712
4	Plasma etch process in a single inter-level dielectric etch	438/689	438/710; 438/712
5	Non metallic barrier formations for copper damascene type interconnects	438/637	438/622; 438/687
6	Process flow to optimize profile of ultra small size photo resist free contact	438/637	438/975
7	Plasma etch process in a single inter-level dielectric etch	438/714	438/719; 438/723; 438/724; 438/725; 438/736
8	Use of boron carbide as an etch-stop and barrier layer for copper dual damascene metallization	438/638	438/624; 438/637; 438/687
9	Process for forming an integrated contact or via	438/637	438/681; 438/712
10	Via patterning for poly(arylene ether) used as an inter-metal dielectric	438/725	216/49; 438/743

	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1		Zheng, Tammy et al.	☒	☐	☐	☐	☐	☐	☐
2		Kitagawa, Hideo	☒	☐	☐	☐	☐	☐	☐
3		Seta, Shoji et al.	☒	☐	☐	☐	☐	☐	☐
4		Tang, Betty et al.	☒	☐	☐	☐	☐	☐	☐
5		Chooi, Simon et al.	☒	☐	☐	☐	☐	☐	☐
6		Tsai, Ming-Huan et al.	☒	☐	☐	☐	☐	☐	☐
7		Tang, Betty et al.	☒	☐	☐	☐	☐	☐	☐
8		Han, Licheng M. et al.	☒	☐	☐	☐	☐	☐	☐
9		Chen, Chao-Cheng et al.	☒	☐	☐	☐	☐	☐	☐
10		Jang, Syun-Ming et al.	☒	☐	☐	☐	☐	☐	☐

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1	US 20010012690	☐
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7	US 6399511	☐
8	US 6352921	☐
9	US 6319822	☐
10	US 6114253	☐

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1	316	438/637,623,700,710,725,780,798.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)	USPAT; US-PGPUB	2002/08/23 13:29
2	288	(438/637,623,700,710,725,780,798.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)) and (via or hole or opening or recess or trench)	USPAT; US-PGPUB	2002/08/23 13:40
3	279	((438/637,623,700,710,725,780,798.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)) and (via or hole or opening or recess or trench)) and @ad<=20010828	USPAT; US-PGPUB	2002/08/23 13:30
4	95	(((438/637,623,700,710,725,780,798.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)) and (via or hole or opening or recess or trench)) and @ad<=20010828) and RF	USPAT; US-PGPUB	2002/08/23 13:37
5	90	257/642,774,758.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)	USPAT; US-PGPUB	2002/08/23 13:30
6	83	(257/642,774,758.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)) and (via or hole or opening or recess or trench)	USPAT; US-PGPUB	2002/08/23 13:30
7	71	((257/642,774,758.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)) and (via or hole or opening or recess or trench)) and @ad<=20010828	USPAT; US-PGPUB	2002/08/23 13:39
8	23	(((257/642,774,758.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)) and (via or hole or opening or recess or trench)) and @ad<=20010828) and RF	USPAT; US-PGPUB	2002/08/23 13:31
9	2	(((438/637,623,700,710,725,780,798.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)) and (via or hole or opening or recess or trench)) and @ad<=20010828) and (RF with sputter with clean)	USPAT; US-PGPUB	2002/08/23 13:38
10	2	(438/637,623,700,710,725,780,798.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)) and (RF with sputter with clean)	USPAT; US-PGPUB	2002/08/23 13:39
11	0	(257/642,774,758.ccls. and (plasma with etching) and ((organic or polymer) same dielectric)) and (RF with sputter with clean)	USPAT; US-PGPUB	2002/08/23 13:39
12	50	(RF with sputter with clean)	USPAT; US-PGPUB	2002/08/23 13:44
13	48	((RF with sputter with clean)) and @ad<=20010828	USPAT; US-PGPUB	2002/08/23 13:39
14	36	(((RF with sputter with clean)) and @ad<=20010828) and (via or hole or opening or recess or trench)	USPAT; US-PGPUB	2002/08/23 13:44
15	17	(RF with sputter with clean)	EPO; JPO; DERWENT; IBM_TDB	2002/08/23 13:44
16	4	((RF with sputter with clean)) and (via or hole or opening or recess or trench)	EPO; JPO; DERWENT; IBM_TDB	2002/08/23 13:44

DOCUMENT-IDENTIFIER: US 20010005635 A1

TITLE: Ashing method and method of producing wired device

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For ashing without degradation of film quality of an **organic** low-dielectric-constant film of a base, there is provided a method of ashing an **organic** resist pattern formed on an interlayer insulating film, which includes an **organic** low-dielectric-constant film at least in part over an article, wherein the ashing is carried out using a plasma of a mixed gas of oxygen and nitrogen. The mixing ratio of nitrogen and oxygen is determined such that the content of oxygen is greater than 0 vol % and not more than 10 vol %.

[0002] The present invention relates to ashing technology for removing an **organic** resist pattern after use and, more particularly, to an ashing method and a method of producing a wired device, which are capable of ashing the **organic** resist pattern whose base is an interlayer insulating film including an **organic** film of a low dielectric constant (hereinafter referred to "**organic** low-dielectric-constant film"), without degradation of the quality of the **organic** low-dielectric-constant film.

[0005] The conventional ashing of a resist pattern on an interlayer insulating film including an **organic** low-dielectric-constant film was conducted mainly using an oxygen plasma. For example, Japanese Patent Application Laid-Open No. 9-153483 discloses a method of carrying out ashing at a good selectivity

between a resist and an **organic** low-dielectric-constant film by cooling a substrate to below room temperature, using an oxygen plasma. This method utilizes a difference in the activation energy of a reaction to oxygen radical between the resist and the **organic** low-dielectric-constant film.

[0006] FIG. 1 shows an example of temperature dependency of ashing rate by an oxygen plasma of a resist and an **organic** low-dielectric-constant film. FIG. 1 is a so-called Arrhenius's plot in which the axis of abscissa indicates 1000/T (T is absolute temperature (K)) and the axis of ordinate the ashing rate (in logarithmic representation), for obtaining the activation energy. When determined using the data shown in FIG. 1, the activation energy of ashing of the resist by the oxygen plasma is 0.17 eV, while the activation energy of the **organic** low-dielectric-constant film is 0.3 eV. Further, the selectivity of a resist to an **organic** low-dielectric-constant film at room temperature (=ashing rate of resist/ashing rate of **organic** low-dielectric-constant film) is approximately 6, and the substrate needs to be cooled to substrate temperatures of -50.degree. C. or less in order to achieve the selectivity of not less than 10. Further, since the ashing rate of an **organic** low-dielectric-constant film is about 40 nm/min to 50 nm/min even below room temperature, the amount of loss of the **organic** low-dielectric-constant film is non-negligible. Further, since the process is carried out in an oxygen plasma, oxygen atoms will diffuse into the **organic** low-dielectric-constant film, while the film is ashed by a small amount. This oxygen may be desorbed during a subsequent film-forming process to cause abnormal film formation.

[0007] In order to solve the above problem, Japanese Patent Application
Laid-Open No. 10-209118 discloses the method of carrying out ashing by a plasma
of a mixed gas of nitrogen and hydrogen. Since this method does not use
oxygen, it is completely free of the degradation of film quality due to the
diffusion of oxygen atoms into the **organic** low-dielectric-constant film. This
method, however, needs to use the hydrogen gas, which is a combustible gas, and
thus handling of the gas is not easy. Further, an apparatus for this method
also needs to be equipped with some explosion-proof means, which adds
complexity to the structure of apparatus. It is also possible to use ammonia
(NH.sub.3) or hydrazine (N.sub.2H.sub.4) instead of hydrogen, but these gases
possess toxicity and thus need to be handled with more care than hydrogen.

[0008] As described above, in the ashing of a resist above an **organic**
low-dielectric-constant film with an oxygen plasma, considerably low
temperatures are necessary for attainment of a high selectivity and thus the
cooling system becomes large in scale.

[0009] In addition, oxygen will inevitably diffuse into the **organic**
low-dielectric-constant film and, for example, if the subsequent step is a
film-forming process of a tungsten plug, abnormal film formation will occur
because of the desorption of the oxygen during the film-forming process.

[0010] An object of the present invention is to provide an ashing method and a
production method of a wired device that are capable of removing a resist
pattern and a side-wall-protecting film remaining after etching by adding a
small amount of oxygen to nitrogen so as to keep the

selectivity high with
regard to an **organic** low-dielectric-constant film.

[0011] FIG. 1 is a graph showing the substrate temperature dependency of ashing
rates of an **organic** low-dielectric-constant film and a photoresist;

[0012] FIGS. 2A, 2B, 2C and 2D are views showing the process flow of etching of
an **organic** low-dielectric-constant film;

[0013] FIGS. 3A and 3B are diagrams showing the structural formulas of **organic**
low-dielectric-constant films used in the present invention; and

[0014] FIG. 4 is a graph showing gas ratio dependency of ashing rates of an
organic low-dielectric-constant film and a photoresist in the gas system of the
present invention.

[0016] A wire 304, an **organic** low-dielectric-constant film 303, and an
inorganic insulating film 302 are formed over a substrate such as a silicon
wafer or the like. Here the wire 304 may be a metal containing at least one
selected from Cu, Al, W, Ti, Ta, and so on, or a nitride or a silicide of the
metal. The **organic** low-dielectric-constant film 303 is an **organic** insulator
(**organic dielectric) having a dielectric** constant (or permittivity or relative
permittivity) lower than SiO.sub.2 and is preferably polyaryl ether or
polyfluoroaryl ether having the structure as illustrated in FIG. 3A or 3B.

[0027] FIG. 4 shows the gas ratio dependency of ashing rates of a photoresist
and an **organic** low-dielectric-constant film in an N.sub.2/O.sub.2-based plasma.
The axis of abscissa indicates the ratio (proportion) of oxygen in a mixture of
nitrogen and oxygen by volume percentage. As is seen from

FIG. 4, the ashing rates of the photoresist and the **organic** low-dielectric-constant film both are 0 at the oxygen ratio of 0 vol %, i.e., without addition of oxygen. With increase in the oxygen ratio, the ashing rate of the **organic** low-dielectric-constant film gradually increases, reaches a maximum at the oxygen ratio of about 20 vol %, and then gradually decreases thereafter. On the other hand, the photoresist demonstrates such complicated behavior that the ashing rate thereof rapidly increases with addition of oxygen even in small ratios of 1 to 3 vol %, reaches a maximum at the oxygen ratio of about 10 vol %, gradually decreases down to a minimum at the oxygen ratio of about 50 vol %, and thereafter increases until the oxygen ratio of 100 vol % is reached. High selectivities for the resist (the ashing rate of the resist/the ashing rate of the **organic** low-dielectric-constant film) are attained when the oxygen ratio is 100 vol % and when a small amount of oxygen is added to nitrogen. When the oxygen ratio is 100 vol %, the selectivity is about 7, so as to accomplish both the relatively high ashing rate and selectivity. However, the ashing rate of the **organic** low-dielectric-constant film is considerably high, about 30 nm/min, and will cause the so-called poisoned via, which is the phenomenon that the **organic** low-dielectric-constant film exposed in the side wall of a via hole is etched in the lateral direction. Further, since the ashing is carried out under the condition of high oxygen ratio, degradation of film quality will occur because of oxygen taken into the **organic** film and abnormal embedding of a metal wire into the hole will further occur in the subsequent film-forming step because of desorption of the oxygen taken into the film.

[0028] On the other hand, since the oxygen ratios are small under the condition of addition of oxygen in small amounts, the above problem of degradation of film quality will not arise at all. Further, there is also the advantage that controllability is very high over occurrence of a poisoned via, because the ashing rates of the **organic** low-dielectric-constant film are very small, not more than 10 nm/min. Under the condition of addition of oxygen 3 vol %, the ashing rate of the resist is considerably low, about 80 nm/min. However, since only small amounts of the photoresist mask and the side-wall-protecting films remain on the substrate surface after the etching of the **organic** low-dielectric-constant film, as also shown in FIG. 2C, the residues can be removed in a short period of time even at a low ashing rate. Therefore, the content of oxygen is preferably higher than 0 vol % and not more than 10 vol %. The content of oxygen is more preferably 3 vol % to 10 vol %.

[0030] The first example of the present invention is an example using FLARE (trade name) available from Allied-Signal Inc., as the **organic** low-dielectric-constant film 303. First prepared was a silicon wafer having the cross-sectional structure illustrated in FIG. 2A. The thicknesses of the respective films were as follows: the thickness of the **organic** low-dielectric-constant film 303 was 700 nm; the thickness of the SiO.sub.2 film 302 was 200 nm; the thickness of the photoresist mask 301 was 670 nm. The photoresist mask 301 was patterned so as to form holes of 0.2 .mu.m throughout in the surface of the wafer. The wafer was set in an **etching** system (not shown) equipped with a surface-wave interfered plasma (hereinafter referred to

as SIP) source such as described in Japanese Patent Application Laid-Open No. 11-40397. Then the inside of the processing chamber was evacuated to 1.times.10.sup.-3 Pa and thereafter reactive ion etching of the SiO.sub.2 film as the hard mask was conducted. The etching conditions were as follows.

[0034] **RF** bias power to substrate: 350 W

[0036] After completion of the etching of the SiO.sub.2 film, the inside of the processing chamber was evacuated to 1.times. 10.sup.-3 Pa and thereafter reactive ion etching of the **organic** low-dielectric-constant film 303 was carried out. The etching conditions were as follows.

[0040] **RF** bias power to substrate: 450 W

[0041] The etching was continued under the above conditions for sixty seconds to remove all of portions of the **organic** low-dielectric-constant film not covered by the mask. The end point of the etching was determined with emission of CN (wavelength: 388 nm) and from intensity of the emission. After completion of the etching, the wafer surface was checked by means of an SEM with the result that a small amount of the photoresist remaining on the surface of the hard mask and the side-wall-protecting films deposited inside the holes were observed.

[0051] The second example of the present invention is an example using SiLK (trade name) available from The Dow Chemical Co., as the **organic** low-dielectric-constant film 303. First prepared was a silicon wafer having the cross-sectional structure illustrated in FIG. 2A, as in Example 1. The thicknesses of the respective films were as follows: the thickness of the

organic low-dielectric-constant film 303 was 600 nm; the thickness of the SiO.sub.2 film 302 was 200 nm; the thickness of the photoresist mask 301 was 670 nm. The photoresist mask 301 was patterned so as to form holes of 0.2 .mu.m throughout in the surface of the wafer. The wafer was set in an etching system (not shown) equipped with the SIP. Then the inside of the processing chamber was evacuated to 1.times.10.sup.-3 Pa and thereafter reactive ion etching of the SiO.sub.2 film as the hard mask was conducted. The etching conditions were as follows.

[0055] **RF** bias power to substrate: 350 W

[0057] After completion of the etching of SiO.sub.2, the inside of the processing chamber was evacuated to the vacuum of 1.times.10.sup.-3 Pa and thereafter the etching of the **organic** low-dielectric-constant film was carried out. The etching conditions were as follows.

[0061] **RF** bias power to substrate: 450 W

[0062] The reactive ion etching was continued under the above conditions for fifty seconds to remove all of portions of the **organic** low-dielectric-constant film not covered by the mask. The end point of the etching was determined with emission of CN (wavelength: 388 nm) and from intensity of the emission. After completion of the etching, the wafer surface was checked by means of an SEM with the result that a small amount of the photoresist remaining on the surface of the hard mask and the side-wall-protecting films deposited inside the holes were observed.

[0072] As described above, according to the present invention, by adding a small amount of oxygen to nitrogen, it becomes possible to

remove a resist
pattern and a side-wall protecting film after etching
substantially with no
etching of an **organic** low-dielectric-constant film.

US-PAT-NO: 6204550

DOCUMENT-IDENTIFIER: US 6204550 B1

TITLE: Method and composition for reducing gate oxide damage during **RF sputter clean**

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Method and composition for reducing gate oxide damage during **RF sputter clean**

Provided is a method and composition for RF sputter cleaning of contact and **via** holes which provides substantially uniform charge distribution in the holes and minimizes electron shadowing. This is accomplished by isotropically depositing, such as by PVD, a layer of conductive material at the wafer surface surrounding a **hole** and down the sides of the **hole**. Isotropic deposition is such that in high aspect ratio trenches and holes deposition is heaviest at the top and minimal at the bottom (due to the deposition shadowing effect). The deposited conductive material is preferably a metal that is also used as a liner in the holes prior to depositing the plug material. The conductive material provides path for negative charge otherwise accumulating at the top of a **hole** during RF sputter cleaning to reach the bottom of the **hole** and thereby prevents accumulations of charge of one polarity in and around the **hole**. Thus, the stress on the gate oxide caused by conventional RF sputtering, described above, is relieved.

This invention relates generally to semiconductor processing, and in particular

to contact and **via** holes. More specifically, the invention relates to a method
of reducing gate oxide damage due to radio frequency (RF) sputter cleaning of
high aspect ratio contact and **via** holes.

In semiconductor processing, conductive elements in non-successive layers of
the semiconductor wafer may be connected by contacts or vias. A **via** is a
connection between two metallic features in different layers of a semiconductor
wafer (a "vertical" connection). A contact is a connection between metallic
and non-metal conducting or semiconducting (such as silicon, polysilicon, or
silicide) features in different layers of a semiconductor wafer.

A contact or **via** is typically formed by depositing a conductive material in a
hole etched through a layer of dielectric between the two layers to be
connected (an inter-layer dielectric ("ILD"). An example of a typical process
for forming a contact is shown in FIGS. 1A-D. FIG. 1A shows a portion of a
semiconductor wafer 100 having a feature in a semiconductor layer 102, for
example a polysilicon floating gate, covered by an ILD 104, for example silicon
dioxide (SiO.sub.2). FIG. 1B shows a contact **hole** 106 etched in the ILD 104,
for instance by plasma etching or reactive ion etching (RIE), using conditions
well known in the art. Such a **hole** typically has a high aspect ratio, for
example a depth twice its diameter or width (2:1 aspect ratio). A typical **via**
hole in a 0.35 .mu.m semiconductor device size environment may be about 500 to
1000 nm deep by about 200 to 500 nm in diameter.

In order to provide the best possible connection to the semiconductor layer
102, the contact **hole** 106 is then typically subjected to a cleaning procedure

to remove the native oxide which forms on the semiconductor layer 102 and any polymer residue remaining from the etch chemistry which forms the **hole** 106. This cleaning is typically accomplished by a wet etch process whereby a selectively corrosive liquid, such as hydrofluoric acid (HF) is dispensed into the **hole** and then removed. The cleaned contact **hole** 106 may be coated with a deposited liner material 110, such as tungsten nitride (WN), titanium nitride (TiN) or titanium tungsten (TiW). The liner material 110 is typically anisotropically deposited, for example, by physical vapor deposition (PVD). The liner 110 provides a good base for deposition of a metal plug 108, typically tungsten (W), deposited by chemical vapor deposition (CVD), as shown in FIG. 1C. It also provides a barrier to prevent corrosion or diffusion of metal ions from the contact or **via** metal plug 108 into the layer to be connected 102.

The transistor region is covered by a first layer of ILD 220, on which a first metal layer 230 is deposited and patterned. The first metal layer 230 and floating gate 210, 216 are connected by a contact 225 (including liner 226). The first metal layer is in turn covered by a second layer of ILD 240 (also referred to as inter metal dielectric ("IMD") where the dielectric separates two metal layers), on which a second metal layer 250 is deposited and patterned. The first 230 and second 250 metal layers are connected by a **via** 235 (including liner 236).

Attention has recently been given to the improvement of the process of cleaning contact or **via** holes prior to deposition of contact and **via** materials in order to minimize contact and **via** resistance. Conventional wet

etch cleaning processes have drawbacks including that the etching liquid does not always reach the base of the high aspect ratio contact and **via** holes, and even when it does, it is not always successful in removing contaminants from the holes. Another way to clean contact and **via** holes, which appears to provide improved results is radio frequency (RF) sputtering. However, plasma induced gate oxide damage may result form such conventional RF sputtering.

FIG. 3 shows a portion of a semiconductor wafer 300 having a substrate 301, a gate oxide layer 302, a polysilicon gate layer 303, an ILD layer 304, and a contact **hole** 306. In RF sputtering, the wafer 300 may be biased to a low potential, for example about -50 to -500 V (typically about -200 V) while a high voltage plasma of argon ions (Ar.sup.+) 310 and electrons 312 is produced by treating argon gas with RF energy above the wafer surface. The following RF process conditions are typically used: the power may range from about 20 to 700 W; the argon pressure may range from about 0.05 mtorr to 25 mtorr; the etch time may range from about 0.5 to 100 s.

The argon ions 310 and electrons 312 from the plasma produced by the RF energy are drawn into the **hole** 306 by the low potential. The electrons 312 tend to move randomly, while the argon ions 310 move more directionally. As a result, a non-uniformity tends to develop in the plasma as the top portion 308 of the **hole** 306 and the wafer surface 305 surrounding the **hole** 306 become negatively charged by the impact of electrons 312. The electrical field due to this negative charge produces an electron shadowing effect whereby electrons 312 subsequently moving in the direction of the **hole** 306 are repelled. Thus, the

number of electrons 312 reaching the bottom 307 of the **hole** 306 is greatly reduced. Meanwhile, a much greater number of the positively charged directional argon ions 310 reach the bottom 307 of the **hole** 306. The negative charge at the top 308 of the **hole** 306 is unable to travel through the isolation dielectric layer 304 to neutralize the positive charge at the bottom 307 of the **hole** 306. As a result, an excess of positive charge develops in the bottom 307 of the **hole** 306.

The local electrical potential built-up by the unbalanced distribution of charges at the top 308 and bottom 307 of the **hole** 306 may degrade the gate oxide 302. The accumulated charge in the bottom of **via hole** 306 may be carried through the gate 302 to the gate/gate oxide interface (not shown in FIG. 3). Typical gate oxides include native defects at the substrate/oxide interface and in the body of the gate oxide. These defects do not cause a problem in normal circumstances, however, an accumulation of a large amount of charge of one polarity adjacent to the gate oxide 302, such as occurs with conventional RF sputter cleaning of contact holes, causes migration of these defects which can lead to degradation of the integrity of the gate oxide and ultimately to its failure. Such problems may also be caused in the cleaning of **via** holes where accumulated charge may flow from the bottom of the **via hole** through the underlying metal layer and contact to the gate and gate oxide, for example in the wafer structure show in FIG. 2.

Accordingly, a **RF sputter clean** process which does not produce an unbalanced charge distribution in contact and **via** holes would be desirable.

To achieve the foregoing, the present invention provides a composition and process for RF sputter cleaning of contact and **via** holes which provides substantially uniform charge distribution in the holes and minimizes electron shadowing. This is accomplished by isotropically depositing, such as by PVD, a layer of conductive material at the wafer surface surrounding a **hole** and down the sides of the **hole**. Isotropic deposition is such that in high aspect ratio trenches and holes deposition is heaviest at the top and minimal at the bottom (due to the deposition shadowing effect). The deposited conductive material is preferably a metal that is also used as a liner in the holes prior to depositing the plug material. The conductive material provides path for negative charge otherwise accumulating at the top of a **hole** during RF sputter cleaning to reach the bottom of the **hole** and thereby prevents accumulations of charge of one polarity in and around the **hole**. The repulsion of electrons is also thereby substantially eliminated, allowing more electrons to reach the bottom of the **hole** directly. Thus, the stress on the gate oxide caused by conventional RF sputtering, described above, is relieved.

The invention exploits the normally disadvantageous deposition shadowing effect of isotropic deposition to provide a desired minimal deposition of conductive material in the bottom of a **hole** so that it does not interfere with the cleaning process. The conductive material need not be removed following completion of cleaning since it preferably is composed of the same material used in the **hole** liner and becomes incorporated into the subsequently deposited liner layer.

FIG. 3 depicts a cross-sectional view of a portion of a

conventional
semiconductor wafer illustrating the non-uniform charge distribution and
electron shadowing effects produced by conventional RF sputter cleaning of
contact and **via** holes.

FIG. 5 depicts a flow chart showing the steps of a method of RF sputter
cleaning of contact and **via** holes in accordance with a preferred embodiment of
the present invention.

As described more fully below, the present invention provides a composition and
process for RF sputter cleaning of contact and **via** holes which provides
substantially uniform charge distribution in the holes and minimizes electron
shadowing. This is accomplished by isotropically depositing, such as by PVD, a
layer of conductive material at the wafer surface surrounding a **hole** and down
the sides of the **hole**. Isotropic deposition is such that in high aspect ratio
trenches and holes deposition is heaviest at the top and minimal at the bottom
(due to the deposition shadowing effect). The deposited conductive material is
preferably a metal that is also used as a liner in the holes prior to
depositing the plug material. The conductive material provides path for
negative charge otherwise accumulating at the top of a **hole** during RF sputter
cleaning to reach the bottom of the **hole** and thereby prevents accumulations of
charge of one polarity in and around the **hole**. The repulsion of electrons is
also thereby substantially eliminated, allowing more electrons to reach the
bottom of the **hole** directly. Thus, the stress on the gate oxide caused by
conventional RF sputtering, described above, is relieved.

In the following description, numerous specific details are set forth in order

to fully illustrate preferred embodiments of the present invention. It will be apparent, however, that the present invention may be practiced without limitation to some specific details presented herein. For example, while the description below refers primarily to contact holes, the invention is also applicable to **via** holes and may further be applied to the cleaning of other **trench** elements during semiconductor wafer processing, such as trenches in the local interconnect.

Referring to FIG. 4, the same cross-sectional view of a portion of a semiconductor wafer as shown in FIG. 3 is shown. FIG. 4 shows a portion of a semiconductor wafer 400 having a substrate 401, a gate oxide layer 402, a polysilicon gate layer 403, an ILD layer 404, and a contact **hole** 406. In addition, according to a preferred embodiment of the present invention, after the contact **hole** 406 etching is complete, and before the RF sputter cleaning process begins, a layer of conductive material 420 may be isotropically deposited, for example by PVD, over the field area surrounding the **hole** at the wafer surface 405 and most of the side walls 415, 416 of the contact **hole** 406.

This aspect of the present invention exploits the normally disadvantageous deposition shadowing effect which may result from PVD of a material in a restricted area. The isotropic nature of PVD and the high aspect ratio deposition substrate provided by the contact **hole** 406 causes a deposition shadowing effect which results in substantial coverage at the wafer surface 405 and **hole** side walls 415 near the top of the **hole** 408, but progressively reduced coverage on the lower side walls 416 and the bottom of a **hole** 407 due to

obstruction of deposition by the high facing side walls.

The conductive layer 420 may be preferably composed of PVD Ti or TiN, particularly where the metal plug is composed of aluminum or an aluminum alloy. The conductive layer 420 may also be composed of PVD Ta, TaN, WN or TiW, for example, particularly where the metal plug is composed of copper, or other suitable materials. The conductive layer material is preferably selected to provide an effective diffusion barrier for the plug material. Preferably the conductive layer will have a thickness of about 20 to 1000 .ANG.; more preferably about 50 to 300 .ANG., and most preferably about 150 .ANG. at the wafer surface 305, gradually reducing to preferably about 50 to 0 .ANG. more preferably about 20 to 0 .ANG., and most preferably about 0 .ANG. at the bottom of the **hole** 406 due to PVD deposition shadowing. PVD process conditions for the conductive layer deposition may be as follows: power about 100 W to 15 kW; pressure about 0.1 mtorr to 200 mtorr.

As in the conventional process, the argon ions 410 and electrons 412 from the plasma produced by the RF energy are drawn by the low potential, and the electrons 412 tend to impact at the surface 405 and near the top 408 of the **hole** 406, while the argon ions 410 reach the bottom 307 of the **hole** 306. However, the presence of the conductive layer 420 provides a path for electrons to flow from the top 408 of the **hole** and the wafer surface 405 surrounding the **hole** 406 to the bottom 407 of the **hole** 406. The repulsion of electrons is also thereby substantially eliminated, allowing more electrons to reach the bottom of the **hole** directly. As a result, positive charges resulting from argon ion 412 impact in the bottom 407 of the **hole** 406 may be

neutralized by the
electrons flowing from the top 408 of the **hole** 406 through the conductive layer
420 and more electrons directly impacting the bottom 407 of the **hole** 406.
Therefore, the conductive layer 420 substantially reduces the electron shading
effect and the effect of the non-uniform plasma environment associated with
conventional RF sputter cleaning, and thus reduces the resulting plasma-induced
damage to the gate oxide 402.

Due to the anisotropic etch nature of the **RF sputter clean** process, the bottom
407 of the **hole** 406, where little or no conductive layer 420 is deposited, may
be cleaned while the conductive layer 420 which coats the rest of the **hole** 406
and surrounding wafer surface 405, maintains the charge balance. Generally,
the conductive layer deposition and **RF sputter clean** processes are preferably
optimized so that the conductive layer's coverage will be substantially
maintained during entire cleaning process. The remaining conductive material
need not be removed following completion of cleaning since it preferably is
composed of the same material used in the **hole** liner and becomes incorporated
into the subsequently deposited liner layer (not shown). Following deposition
of the liner, the remainder of the **hole** may be filled with conductive material
(not shown), preferably a metal, that is compatible with the liner material, as
described above.

FIG. 5 shows a flow chart 500 of a preferred method of cleaning a contact or
via hole, in accordance with a preferred embodiment of the present invention.
The method 500 begins at 501, and at a step 502 a semiconductor wafer having a
contact or **via hole** in its surface is provided. At a step 504, a layer of

conductive material is isotropically deposited on the wafer surface surrounding the **hole and in the hole**. Preferably, conductive material is also suitable as a liner for the **hole,** for example Ti or TiN. A preferred deposition method for the material is by sputtering (PVD). Such isotropic deposition in a high aspect ratio holes result in decreased deposition towards the bottom of the **hole**.

At a step 506, the **hole** is cleaned using an RF sputter cleaning process, such as described above. This process is preferably optimized so that the conductive layer's coverage will be substantially maintained during entire cleaning process. The process ends at 508.

As described above, the remaining conductive material need not be removed following completion of cleaning since it preferably is composed of the same material used in the **hole** liner and becomes incorporated into the subsequently deposited liner layer (not shown). Following deposition of the liner, the remainder of the **hole** may be filled with conductive material (not shown), preferably a metal, that is compatible with the liner material.

1. A composition for balancing charge during RF sputter cleaning of a **hole** for electrically connecting two conductive features in non-successive layers of a semiconductor wafer, comprising:

a **hole** in a dielectric surface layer of a semiconductor wafer; and

an isotropically deposited layer of electrically conductive material in said **hole,** said layer gradually decreasing in thickness to about 50 to 0 .ANG. at the bottom of said **hole**.

2. The composition of claim 1 wherein said **hole** is a contact **hole**.

3. The composition of claim 1 wherein said **hole is a via hole**.

4. The composition of claim 1 wherein said **hole** has about a 2:1 aspect ratio.

8. The composition of claim 1 wherein said electrically conductive material
has a thickness of about 20 to 1000 .ANG. at the wafer surface, gradually
reducing to about 50 to 0 .ANG. at the bottom of the **hole**.

9. The composition of claim 8 wherein said electrically conductive material
has a thickness of about 50 to 300 .ANG. at the wafer surface, gradually
reducing to about 20 to 0 .ANG. at the bottom of the **hole**.

10. The composition of claim 9 wherein said electrically conductive material
has a thickness of about 150 .ANG. at the wafer surface, gradually reducing to
about 0 .ANG. at the bottom of the **hole**.

11. The composition of claim 1 wherein coverage of the electrically conductive
layer from the top the bottom of the **hole** is substantially maintained during
cleaning.

DOCUMENT-IDENTIFIER: NN84014280

TITLE: Plasma Etching of Polyimide Through an Aluminum Mask

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- Plasma etching of polyimide through an aluminum mask in an oxidizing atmosphere enables the entire mask to be converted to oxide and removed by a back door etch process. Alternatively, the thickness of aluminum can be increased so that some metal remains to protect the polyimide during subsequent RF sputter cleaning and to enable direct deposition of second level aluminum metallization. As shown in Fig. 1, an aluminum mask 10 of around 250-400 A thickness is used to define **via** holes 11 through a polyimide insulation layer 12 to enable contact with a first level aluminum metallization level 13 on the surface of wafer 9. Both aluminum layers are covered with thin layers 14 and 15 of native oxide. During plasma etching in an oxidizing atmosphere the oxide thickness in layer 10 is increased until all or most of the mask is converted to oxide. Both the mask and the native oxide can now be removed together by a so-called "back door etch" process in an aqueous solution of ammonium phosphate. As an alternative, where a second level of metallization is required, the thickness of layer 10 can be increased to 400-700 A . In this case, as shown in Fig. 2, not all the mask is converted to oxide and aluminum remains on the surface after the back door etch. This aluminum is used to protect the polyimide from surface damage during **RF sputter clean** prior to second level

metallization. The aluminum
also maintains the front surface of the wafer at a uniform
potential, thereby
preventing electron damage to underlying FETs. The
structure is then as shown
in Fig. 3. Second level aluminum can then be deposited
directly over the
protective mask, and the two layers sintered to remove the
interface between
them.

FIG. 1

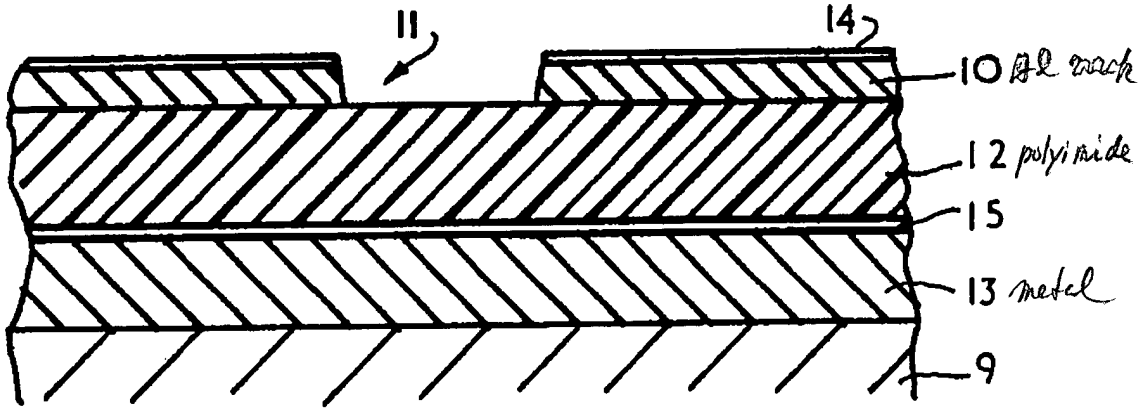

FIG. 2

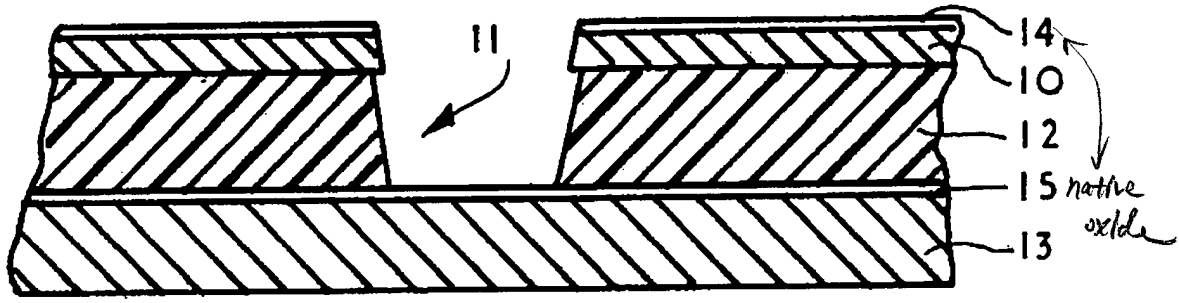

FIG. 3